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4 / IDS  
E. Willis  
11-15-01

Our Case No.: 10519/30  
MA-001-I-b

U.S. PTO  
09/939498  
02/08/24/01  
JG986

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Subramanian et al.

Serial No.: Unassigned

Filing Date: Filed herewith

For: VERTICALLY STACKED FIELD  
PROGRAMMABLE NONVOLATILE  
MEMORY AND METHOD OF  
FABRICATION

Examiner: Unassigned

Group Art Unit No.: Unassigned

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed below and on the attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents required by 37 C.F.R. § 1.98(a)(2) are enclosed for the convenience of the Examiner.

The references now cited are the following:

No.	Date	Name
4,272,880	6/16/1981	Pashley
4,442,507	4/10/1984	Roesner
4,489,478	12/25/1984	Sakurai
4,498,226	2/12/1985	Inoue et al.
4,499,557	2/12/1985	Holmberg et al.
4,646,266	2/24/1987	Ovshinsky et al.
4,677,742	7/7/1987	Johnson

5,070,384	12/3/1991	McCollum et al.
5,306,935	4/26/1994	Esquivel et al.
5,427,979	6/27/1995	Chang
5,441,907	8/15/1995	Sung et al.
5,602,987	2/11/1997	Harari et al.
5,640,343	6/17/1997	Gallagher et al.
5,745,407	4/28/1998	Levy et al.
5,835,396	11/10/1998	Zhang
5,929,478	7/27/1999	Parris et al.
5,969,383	10/19/1999	Chang et al.
6,034,882	3/7/2000	Johnson et al.

#### FOREIGN DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY
WO 99/14763	3/25/1999	WIPO

#### OTHER ART

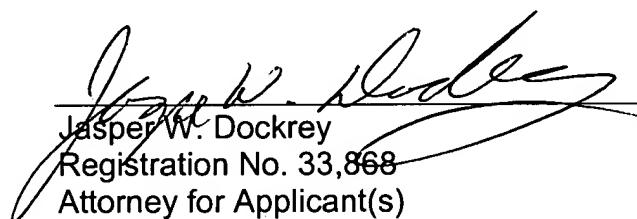
1. John H. Douglas, "The Route to 3-D Chips", *High Technology*, 3, No. 9, 55-59 (1983)
2. Kawashima et al., "A Charge-Transfer Amplifier and an Encoded-Bus Architecture for Low-Power SRAM's", *IEEE Journal of Solid-State Circuits*, 33, No. 5, 793-799 (1998)
3. Cappelletti et al., "Flash Memories", Kluwer Academic Publishers, Table of Contents, pp. 47, pp. 308 (1999)
4. "Three-Dimensional Read-Only Memory (3D-ROM)" [online] [retrieved on 8/10/00] retrieved from the Internet: <URL: <http://sites.netscape.net/zhangpatents/3D-ROM/3D-ROM.htm>
5. Semiconductor International, "3D-ROM-A First Practical Step Towards 3D-IC" [online] [retrieved on 8/10/00] retrieved from the Internet: <URL: <http://www.semiconductor.net/semiconductor/Issues/webexclusives/200.../six00063DROM.as>

In accordance with 37 C.F.R. § 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed to be an admission that the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

This Information Disclosure Statement is being filed prior to the receipt of the first Official Action reflecting an examination on the merits and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these material, the Commissioner is hereby authorized to deduct said fees from Brinks Hofer Gilson & Lione Deposit Account No. 23-1925. A duplicate copy of this document is enclosed.

Applicant(s) respectfully request that the listed documents be made of record in the present case.

Respectfully submitted,



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